REMARKS

In the Official Action mailed 29 December 2005 claims 1-65 were indicated as being rejected pursuant to 35 U.S.C. §103(a). However, only claims 1-64 are pending in the application. Therefore, Applicants shall interpret the rejection as being directed to claims 1-64. Applicant has amended claims 1, 23 and 45 and canceled claims 5, 28 and 49. Claims 1-4, 6-27 and 29-64 remain pending.

Rejection of Amended Claim 1

Claim 1 was rejected pursuant to 35 U.S.C. §103(a) as allegedly being obvious over Walukas 6,229,737, in view of Kobatake 5,815,441 and Lin 6,671,209. To more clearly distinguish the claimed invention from the cited prior art, Applicants have amended the claims to define an integrated circuit that includes, *inter alia*, a first memory array on a substrate comprising charge storage nonvolatile memory cells configured to store data for a first pattern of data usage in response to a first operation algorithm, with the first memory array including first memory cells having a first cell structure; and a second memory array on the substrate comprising charge storage nonvolatile memory cells configured to store data for a second pattern of data usage and facilitate bit-by-bit erasure of data in the second memory array in response to a second operation algorithm, with the second memory array including second memory cells having a second cell structure that is substantially the same as the first cell structure. Applicants teach this structure in order to provide high-yield low-cost multi-functional memory devices. See ¶ **[0007]**, page 8. To that end, two memory arrays are formed on a single die having a common cell structure with differing operational characteristics. See *id*. Providing the cell structures of the differing arrays with a common structure reduces the manufacturing complexity while providing multi-functionality. One of the desired functionalities provided by the present invention is bit-by-bit erasure. See ¶ **[0029]** and Tables 1 and 2.

The prior art, on the other hand, is not directed to bit-by-bit access of cells in a memory array as claimed. With reference to the first embodiment his invention, Kobatake teaches that the memory cells in the first and second arrays have similar structures. See col. 4, lines 62-63. However, the first embodiment is discussed with respect to one of the memory arrays being configured for a group-by group erasure, and the second memory array is configured for a batch erasure. See col. 2, lines 41-46; col. 5, lines 25-27; and col. 5, lines 58-63. Kobatake advocate this structure in order to save erasure time. See col. 5, lines 58-63, as well as to ease the cost of

manufacture by fabricating both memory arrays with a common process. See col. 3, lines 1-3. The one embodiment in which Kobatake teaches bit-by-bit erasure, however, Kobatake recites that the floating gates and the control gates in the first nonvolatile memory are larger than the same components in the second memory array. See col. 8, lines 9-14. This differing structure between the cells of the two memory arrays is described as providing the capacitance between the control gate and the floating gate to provide bit-by-bit erasure. See col. 8, lines 25-28. As a result, it becomes clear that Kobatake teaches away from the claimed integrated circuit in which the memory cells of two differing memory arrays have the same cell structure with one of the memory arrays providing bit-by-bit erasure in the cells.

The remaining prior art does not overcome the deficiencies of Kobatake. Specifically, Walukas teaches using traditional EEPROM and flash memory devices and makes no mention of fabricating the same on a single chip. Moreover, Walukas is completely silent with respect to the erasure operation. Rather, Walukas is directed to efficiently writing to a nonvolatile memory in an efficient manner. See col. 2, lines 41-44. Therefore, Walukas does not recognize the problems faced by Applicants, lower manufacturing costs of nonvolatile memory devices while providing multi-functionality. Without recognizing Applicant's problem, there is no suggestion to modify Walukas to provide Applicant's claimed integrated circuit.

Moreover, Lin does not overcome the deficiencies of either Kobatake or Walukas. Therefore, Applicants respectfully contend that claim 1, as amended, defines an invention suitable for patent protection.

Rejection of Amended Claim 23

Claim 23 was rejected pursuant to 35 U.S.C. §103(a) as allegedly being obvious over Walukas 6,229,737, in view of Kobatake 5,815,441 and Lin 6,671,209. Amended claim 23 defines a method for manufacturing an integrated circuit device that includes, *inter alia*, forming a first memory array on a substrate comprising charge storage, nonvolatile memory cells, configured to store data according to a first pattern of data usage in response to a first operation algorithm. The first memory array includes first memory cells having a first cell structure. A second memory array is formed on the substrate comprising charge storage, nonvolatile memory cells, configured to store data according to a second pattern of data usage and facilitate bit-by-bit erasure of data in the second memory array in response to a second operation algorithm. The

second memory array includes second memory cells having a second cell structure that is substantially the same as the first cell structure.

Applicants submit that the arguments set forth above with respect to amended claim 1 apply with equal weight here with respect to claim 23, as amended. Therefore, Applicants submit that claim 23, as amended, defines a method of manufacturing suitable for patent protection.

Rejection of Amended Claim 45

Claim 45 was rejected pursuant to 35 U.S.C. §103(a) as allegedly being obvious over Walukas 6,229,737, in view of Kobatake 5,815,441 and Lin 6,671,209. Amended claim 45 defines a method for manufacturing an integrated circuit device that includes, *inter alia*, addressing a first memory array comprising nonvolatile memory cells on the integrated circuit, to read, program and erase first data; addressing a second memory array comprising nonvolatile memory cells on the integrated circuit, to read, program and erase second data; reading, programming and erasing first data in the first memory array according to a first operation algorithm adapted for a first pattern of data usage. The first memory array includes first memory cells having a first cell structure; reading, programming and erasing second data in the second memory array occurs according to a second operation algorithm adapted for a second pattern of data usage. The second memory array includes second memory cells having a second cell structure that is substantially the same as the first cell structure, wherein the second operation algorithm is not the same as the first operation algorithm, with erasing said second data occurring bit-by-bit.

Applicants submit that the arguments set forth above with respect to amended claim 1 apply with equal weight here with respect to claim 23, as amended. Therefore, Applicants submit that claim 45, as amended, defines a method of manufacturing suitable for patent protection.

Dependent Claims

Considering that the dependent claims include all of the limitations of the independent claims from which they depend, the dependent claims define inventions suitable for patent protection to the extent the independent claims define inventions suitable for patent protection. Therefore, based upon the foregoing arguments with respect to the independent claims,

Applicants respectfully contend that the dependent claims define subject matter suitable for patent protection.

CONCLUSION

Accordingly, reconsideration of the rejection of claims 1-4, 6-27 and 29-64 as amended is respectfully requested. A notice of allowance is earnestly solicited.

The Commissioner is hereby authorized to charge any fee determined to be due in connection with this communication, or credit any overpayment, to our Deposit Account No. 50-0869 (MXIC 1571-1).

Respectfully submitted,

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